Brendan Lynskey brendanlynskey@googlemail.com

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13 Ivy Grove, Shipley, Bradford. BD18 4JZ

Role **Senior / Principal FPGA Engineer**

Skills

FPGA / SoC Design, (Synopsys, Mentor, Cadence, Xilinx, Altera):

- RTL design, synthesis, layout, timing-closure, IP design
- VHDL, Verilog, SystemVerilog
- CPU, AXI, PCIe, High Speed Serial, DDR2/3, DSP, Datacomms
- Xilinx Certified Engineer; some Altera experience

FPGA / SoC Verification, (Cadence, Mentor, Synopsys , Python, MATLAB):

- Verification plans, transactors, VPI, self-checking TB, coverage

High-Performance Hardware, (Altium, Cadence, Mentor, Visula):

- Design & schematics, layout guidance and review, 6Gbs serial, SI, PI, bring-up/debug, thermal design/test, analogue signal-capture, RF testing

Software:

- C/C++, Python, Perl, Tcl, shell scripts, MATLAB, Java.
- Embedded Linux (U-Boot, Buildroot)
- Worked on multiple OS for multiple architectures

DSP:

- Analysis, verification, and implementation of algorithms. Lots of MATLAB, Simulink and Mathcad

Applications:

- Audio-video, SoC debug tools, Networking (MAC/PHY), Cryptography, Storage, Medical, Geophysics

Other skills: Planning, mentoring, process, Linux sys-admin

Experience

2014-present: Imagination Technologies

Senior Engineer – MIPS

Working in MIPS Business Unit (Tools Group), across the board on RTL, HW, and SW.

Developed high performance debug-probe systems, using Xilinx 7 Series FPGAs, including PCIe bus mastering, AXI, XADC, DDR3, and Aurora IP. Products incorporated analogue signal-capture system; I developed full chain from current-sensing front-end to decimation filter.

Developed SoC core for On Chip Debug (will be used in the iPhone 11!)

Worked on FPGA prototyping platforms for IP cores, debugging existing Xilinx UltraScale based platform, and evaluated new UltraScale+ based platform (AWS EC2 F1): https://aws.amazon.com/ec2/instance-types/f1/

Developed TCP/IP sockets-based verification transactors which enable the use of Codescape SW debugger in verification environments: simulations using Verilog VPI, emulations using DPI/BFMs.

Authored a development-process for HW team.

2011-2014: Red Embedded

Senior Consultant – Consultancy group

Working across the board in HW, FPGA and SW, specifically:

- Xilinx FPGA-based Professional Broadcast product (VHDL, C):
  - 8x HDMI in, 8x dual-SDI out, +1 HDMI+SDI ‘mosaic’ monitor output
  - Xilinx Video IP blocks (V-DMA, video scaler, AXI interconnect
  - Atom-based PC running Ubuntu

- PC-based video-processing software project (Python, C++)

- Automated RF test project for Powerline comms (Python)

- Two FPGA DSP projects for Geophysics and Medical applications (Verilog, VHDL, SysGen)

2005-2011: Pace plc

Principal Engineer – Technologies Group, and then Pace Networks

Designed, implemented, and verified many functional modules for Headend/Transmodulator FPGAs, contributing to:

- QPSK/16-QAM DOCSIS burst receiver
- 64/256-QAM J.83 modulator
- Embedded CPU systems using EDK, (Microblaze and PowerPC)
- High-performance packet-classifier/switches, including DDR interfaces, proprietary on-chip bus standard, large FIFO abstraction modules
- Gb Ethernet interface
- High-speed inter-FPGA links

Overhauled group's verification strategy, and then the group's DSP strategy. Responsible for all board-level aspects of FPGA design (pinouts, TX-lines), and other timing aspects (interface function over temperature-ranges, and clock-domain crossings in these multi-FPGA/PCB projects). I also designed and implemented several low-level software modules.

Also whilst at Pace, I successfully designed/verified/implemented MPEG Descrambling FPGA, (triple-DES), and a DVB-S BER tester FPGA.

2002-2005: Comodo Research Lab.

Senior ASIC Engineer – Secure Hardware Department

Worked on all front-end stages of *TCPM4000* 0.18um standard cell SoC, (packaged with EEPROM). Designed/implemented/verified modules and system. Incorporates:

- Original crypto processor: RSA, SHA-1, 3DES, AES, PRNG, (potentially *TPM).* Original Keyboard and I^2C interfaces, RTC, Watchdog, Clocks/resets controller. Digital IP: 8051 CPU, USB, Smartcard and LPC interfaces

Applications: *TPM*, USB-based Security Token/Smartcard Reader/Keyboard Controller.

1998–2002: Pace Micro Technology

Hardware Engineer – Advanced Projects Group

Implemented Pace's first Hard-Disk MPEG-2 prototype, (PCB, FPGA) and DVB and Hard-Disk UDMA-66 blocks in FPGA for 3DES-protected PVR

Implemented Bridge for ADSL-HPNA-Set-Top-Box system, (PCB, FPGA).

Implemented HW and SW for IrDA handset Speech/Speaker Recognition, incorporating an electret microphone, ADC, FPGA, IrDA link, *sockets* application to PC.

Won *Most Inspiring Invention 2000*.

1994–1997: Thales Underwater Systems

Hardware Engineer - Sonar Systems Hardware Department

Rainbow DSP co-processor ASIC (not completed).

Designed to completion the Sonar 2076 *Data Transceiver*, incorporating:

- Fibre-optics running at 1.0625Gbits/s, microstrip and stripline PCB design
- ECL / Pseudo-ECL serial datapath, (with original translator)
- *Fibre-Channel* chipset, FPGAs for network/comms functions, Dual-Port SRAM
- CPLD for CPU interfacing, SHARC Processors, EEPROM, RTC

Education / Training

2008: University of Manchester: M.Sc. Low-Power Systems Integration, (part-time, distance-learning, *DISTINCTION*)

- Analogue/Mixed-Signal/Digital design. Low-Power design.
- IP Block Authoring. Soft/Firm/Hard blocks. Asynchronous Design.
- Embedded SW. Design/implementation, ARM-based systems, (ASM, C).

Project: full development of AMBA Ethernet ASIC core for 130nm Artisan standard-cell library. Executed all tasks: requirements, design, simulation, FPGA emulation, and SW driver development. The core worked first time in Prof. Steve Furber's *SpiNNaker* multiprocessor system

1997–1998: University of York: M.Sc. Music Technology

- DSP, acoustics, sound synthesis and processing
- C programming for DSP
- Sound design, Composition

Project: Discrete wavelet-transform based spectral modification apps, in C on SGI platform.

1991-1994: UMIST: B.Eng. (Hons) Electronic Engineering

- Standard electronics engineering undergraduate syllabus

Project: Computer Arithmetic for an Actel CPLD-based pocket calculator, (using Mentor in VHDL).

Ongoing: Open University: B.Sc. (Hons) Mathematics and Computing

On hold due to arrival of young family, have completed *Diploma in Mathematics* to date (distinctions in modules). Also covered good amount of SW (OO, concurrency, distributed systems, etc.).

Courses completed:

2018: C++ for C programmers (Coursera)

2018: Version control with Git (Coursera)

2017: École Polytechnique Fédérale de Lausanne: Digital Signal Processing (Coursera)

2017: 2x Udemy SystemVerilog Verification courses

2017: Peking University: Chinese for beginners (Coursera)

2017: Stanford University: Machine Learning (Coursera)

2017: University of Toronto: Neural Networks for Machine Learning (Coursera)

2016: Princeton University: Computer Architecture (Coursera)

2016: University of Oxford: Advanced High-Speed Signal Propagation (online)

2016: University of Oxford: High Speed Digital Design (online)

2014: Altera: Video Design Framework Workshop

2010: University of Oxford: Practical RF/Microwave Design

2009: University of Bolton: 3-month postgrad DSP course (grade A)

2008: Xilinx: DSP Implementation Techniques for FPGAs

2008: Excentis: EuroDOCSIS 2.0

2006: Xilinx: Advanced Implementation and Verification course

2004: Synopsys: Physical Compiler course

2001: Doulos : Expert VHDL course

Personal Details

DOB: 14th October, 1972. Nationality: British. Married.

Languages: English and some French and Italian.

I'm enthusiastic and self-motivated. I work well in a team, and strive to be a front-runner. I take pride in doing a good job, from initiation to completion. I'm a thorough planner, and tenacious in all tasks undertaken.

In work I don't confine myself to narrow disciplines: when I find that I don't know something, I learn it. I believe that an engineer should see a project right through to the end, in order to close the corrective feedback loop.

I try to analyse everything I do. I'm very interested in the everyday biases all engineers face, and how judgement can be compromised.

I'm a good communicator: I believe that English is the most important language an engineer should know: we can't do these things alone.

I'm always keen to learn new skills, and to improve my understanding. I love to work, and I always finish projects.

Interests

History of science and engineering.

Mathematics and all its applications in computing (like DSP)

Linux, computer architecture, history of computing.

Reading a wide range of subjects.

Spending time with my family.

Music (listening to and making badly).

Running.

Member of IET.

References:

Available on request.